Research Summary

Changjae Moon

POSTECH
POHANG UNIVERSITY OF SCIENCE AND TECHNOLOGY

Changjae Moon

■ Educaton

- **PostDoc** Pohang University of Science and Technology (POSTECH), Korea Mar. 2025 – Present
- **M.S.-Ph.D Combined** POSTECH, Korea Mar. 2019 – Feb. 2025
- **B.S.** POSTECH, Korea Mar. 2014 – Aug. 2018

■ Reasearch Interests

- Energy-Efficient TRX Archietectures
- Novel Equalization Techniques and Signal Modulations for High-Speed Links
- Optical Modulator Driver Design (Ongoing)

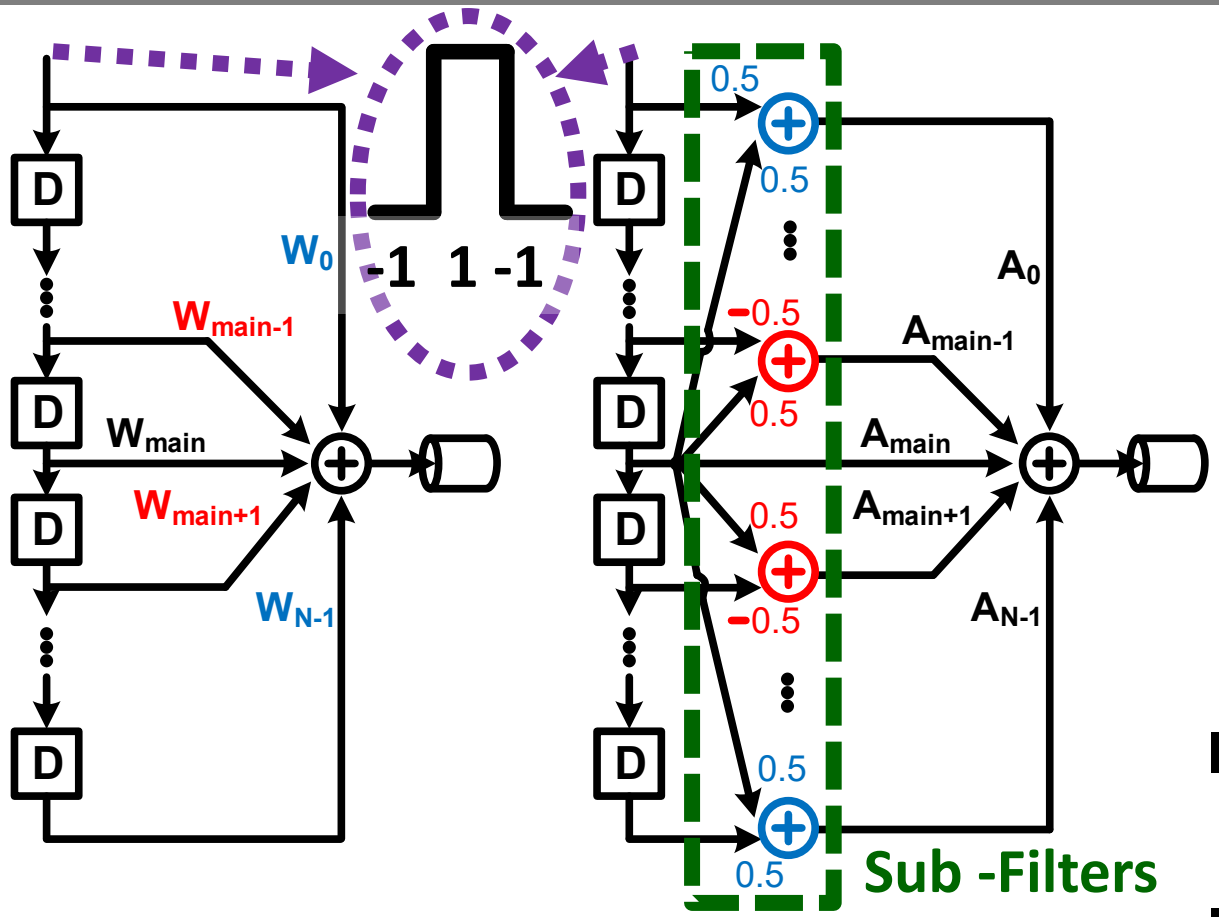
■ Technical Specialties

- Interconnet Modeling and Characterization
- High-Speed I/O Cicuit Design
  - High-Speed TRXs, FFE, DFE, CTLE, PLL, CDR, and Clock Distribution Circuits
- On-Chip Measurement and Testing Methodology

■ Skills

- Programming Languages: C languages and Python
- Cicuit Simulation Tools: HFSS, EMX, Cadence, Verilog, and Matlab & Simulink
- Synthesis Tools: Design compiler and IC compiler
- PCB Tool: PADS

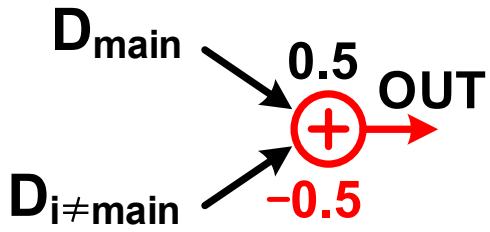
1) Addition-Only FFE (A-FFE) TX



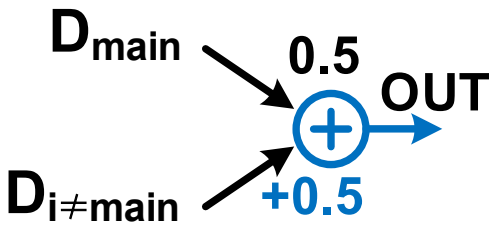
C-FFE **A-FFE**

$$A_{main} = W_{main} - \sum_{\substack{i=0 \\ i \neq main}}^{N-1} |W_i| \quad , \quad A_{i \neq main} = 2|W_i|$$

Difference Filter



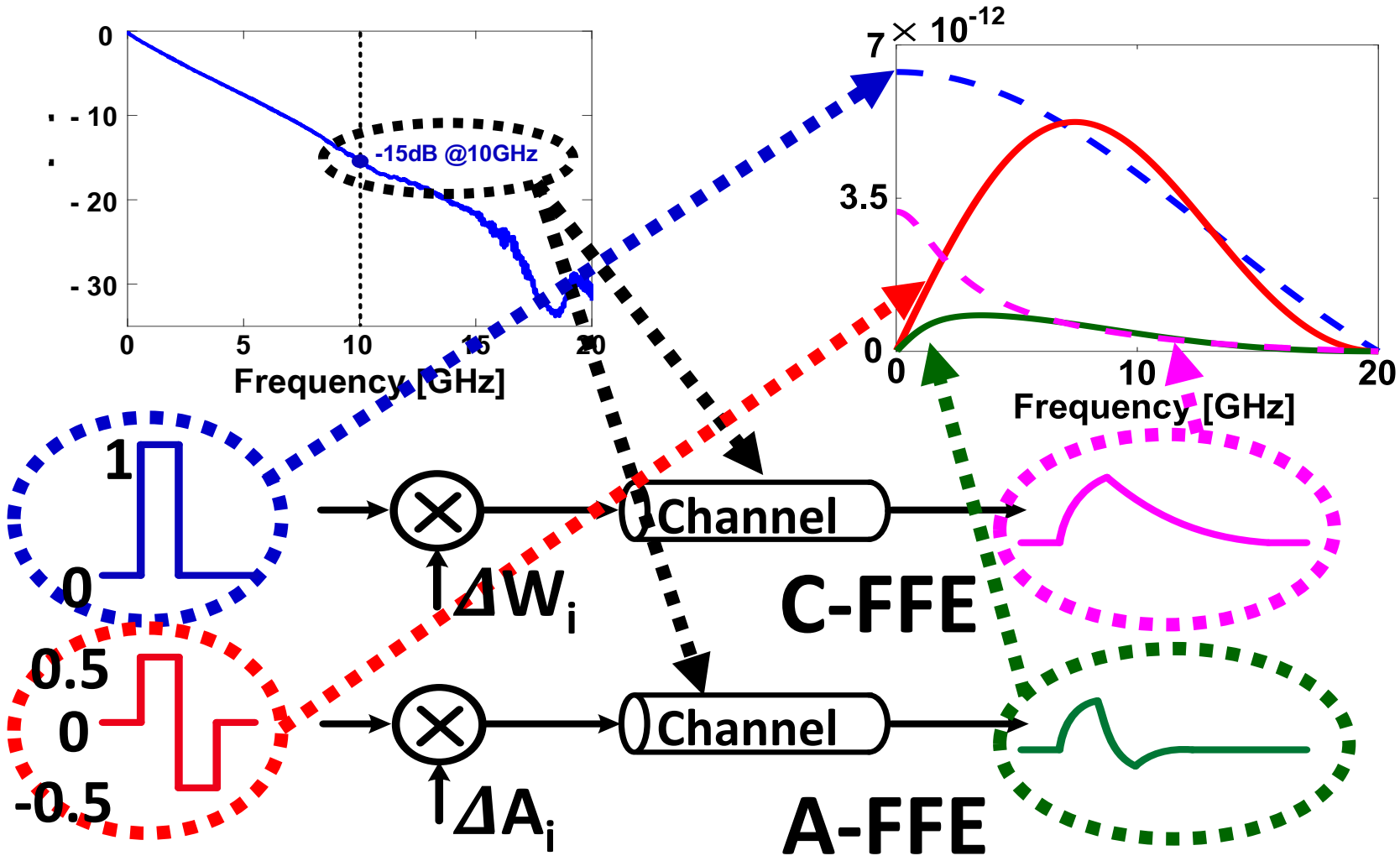
Average Filter



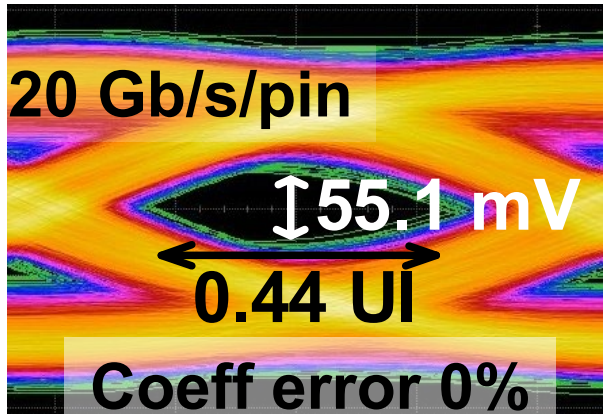
D_i D_{main}	Difference Filter Output	Average Filter Output
-1 -1	0	-1
-1 +1	+1	0
+1 -1	-1	0
+1 +1	0	+1

- In A-FFE, there are **no subtractions** between taps, **only additions**.
- The A-FFE sub-filter is either a **difference filter** or an **average filter**.
- The sub-filter type is determined by **the sign of the CFFE cursor**.

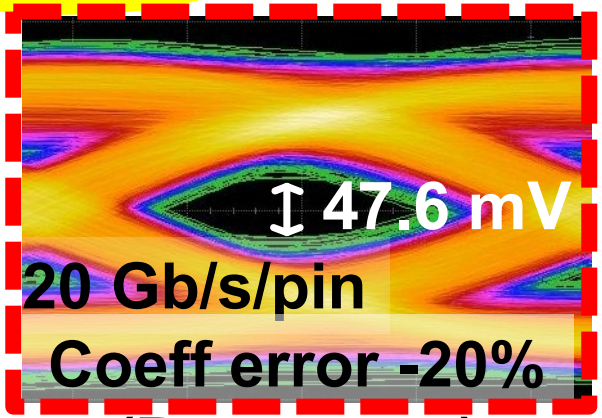
1) Robustness to Errors of Coefficients



Measured Eye Diagram



Worst Case



(Pre-cursor)

- The low pass filter channel attenuate the AFFE's error pulse.

→ At the RX, the impact of the A-FFE coefficient error is attenuated.

1) A-FFE TX

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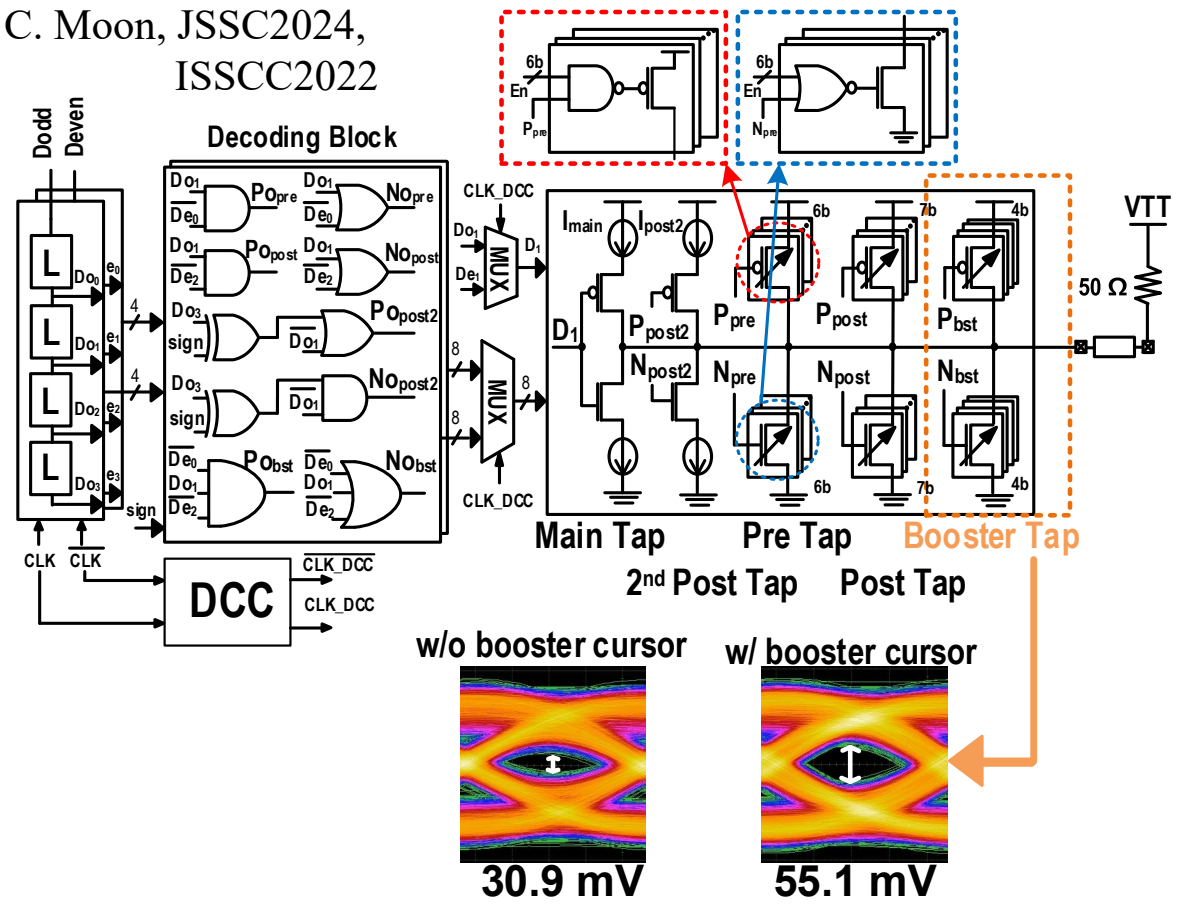
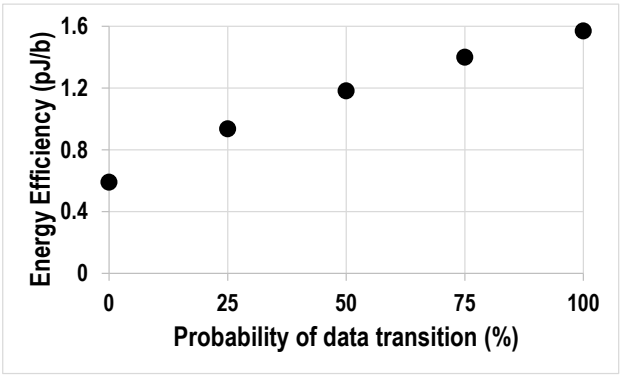
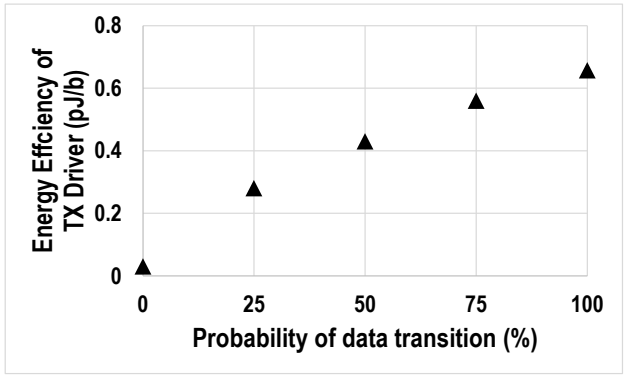
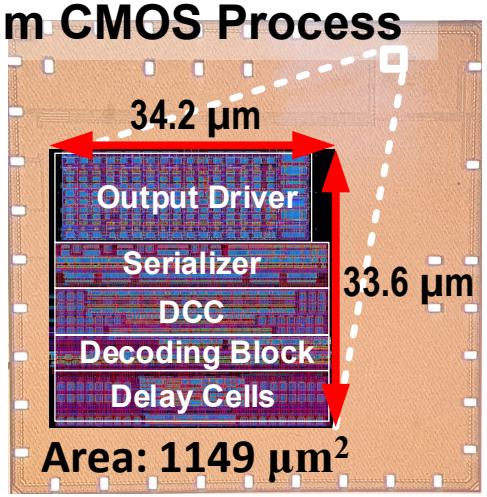
ISSCC2022



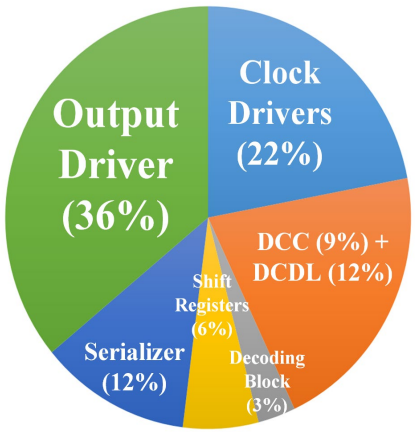




28nm CMOS Process

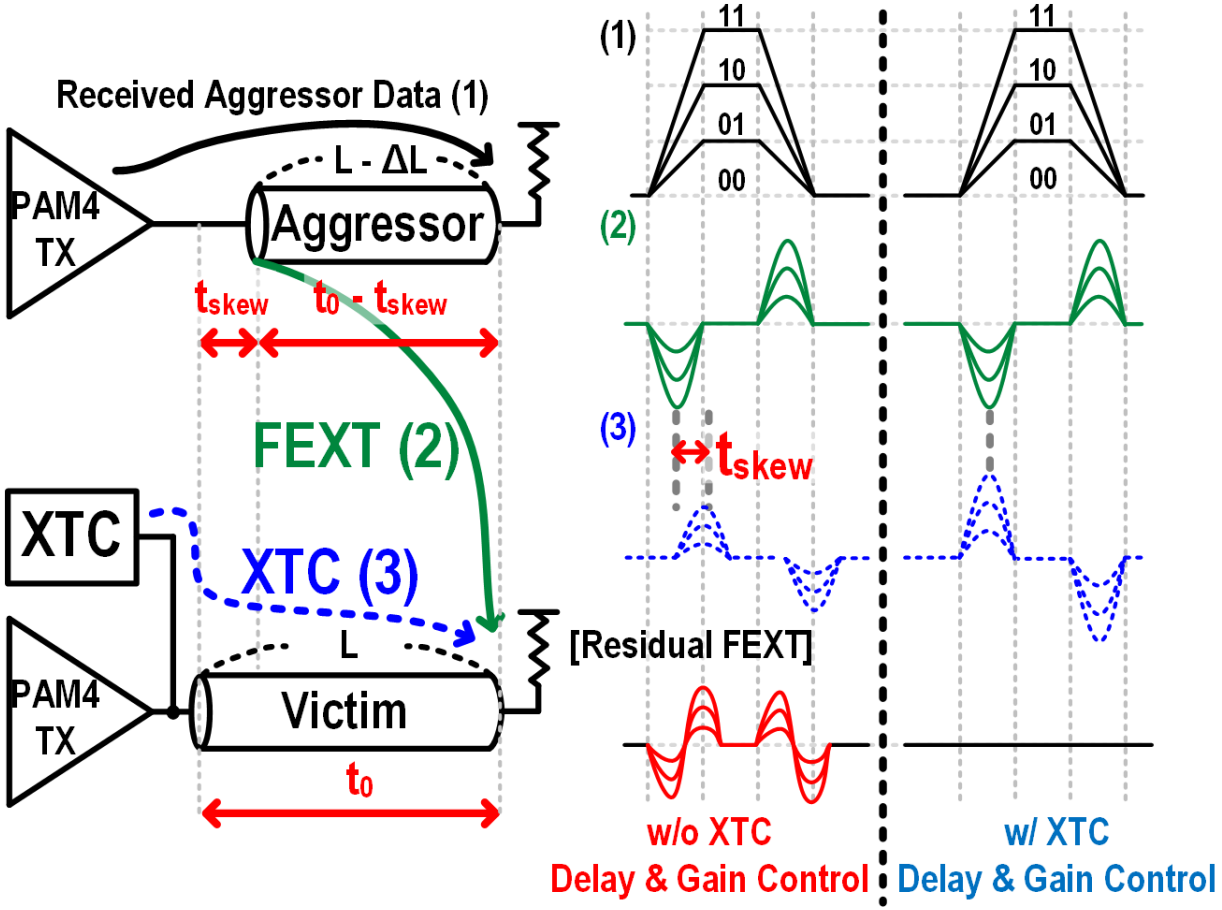


Power Breakdown



- The TX achieved 20 Gb/s/pin with 55.1 mV eye height over 15 dB PCB trace at 1.18 pJ/b.
- Since A-FFE taps activate only when needed, energy scales linearly with transition probability.

2) PAM4 Crosstalk Compensation (PAM4 XTC)



Aggressor

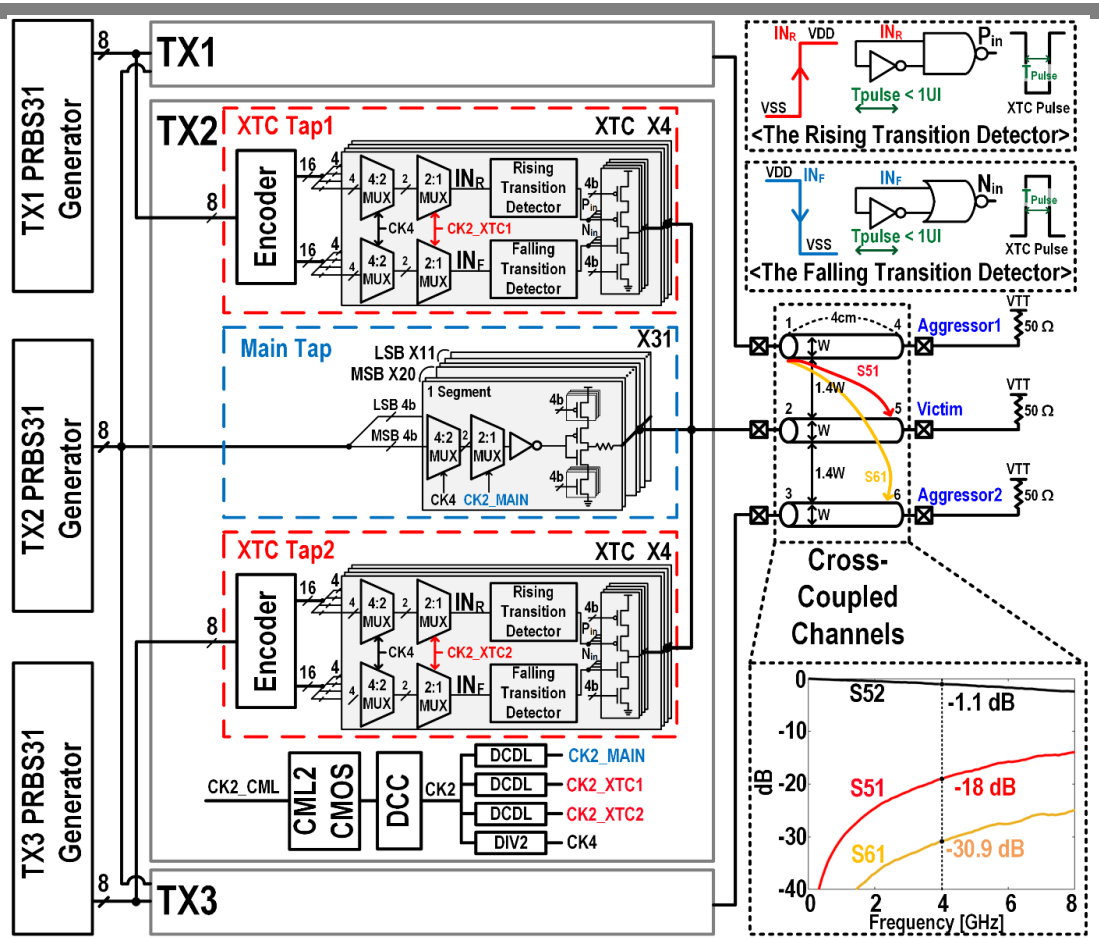
FEXT

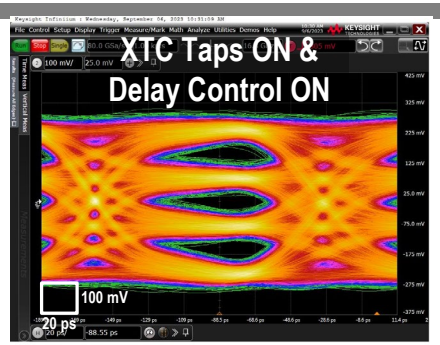
Skewed XTC

RX input of Victim

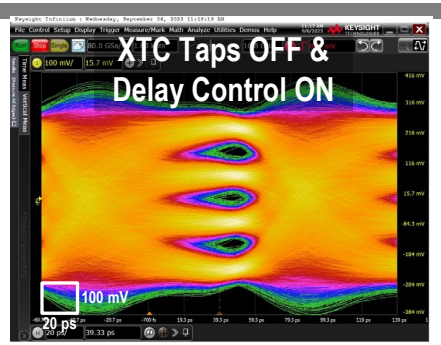
- PAM4 crosstalk amplitude dynamically changes with the data pattern.
- Interconnect skews make crosstalk compensation (XTC) more difficult.

2) PAM4 TXs with Crosstalk Compensation

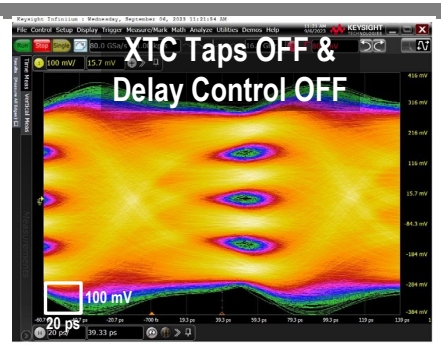




Eye	Width [UI]	Height [mV]
Top	0.352	40.3
Middle	0.384	43.2
Bottom	0.352	60

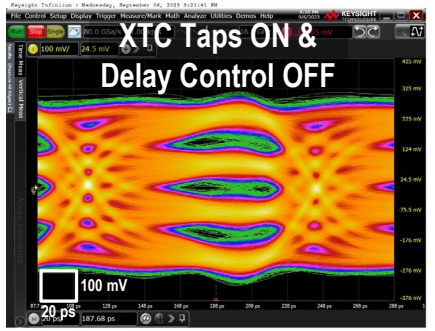


Eye	Width [UI]	Height [mV]
Top	0.107	30.2
Middle	0.071	13.3
Bottom	0.089	26.7

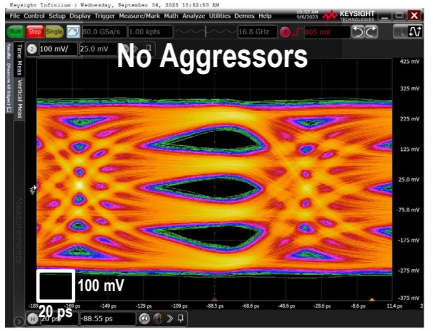


Eye	Width [UI]	Height [mV]
Top	closed	closed
Middle	closed	closed
Bottom	closed	closed

C. Moon, TCASII 2024



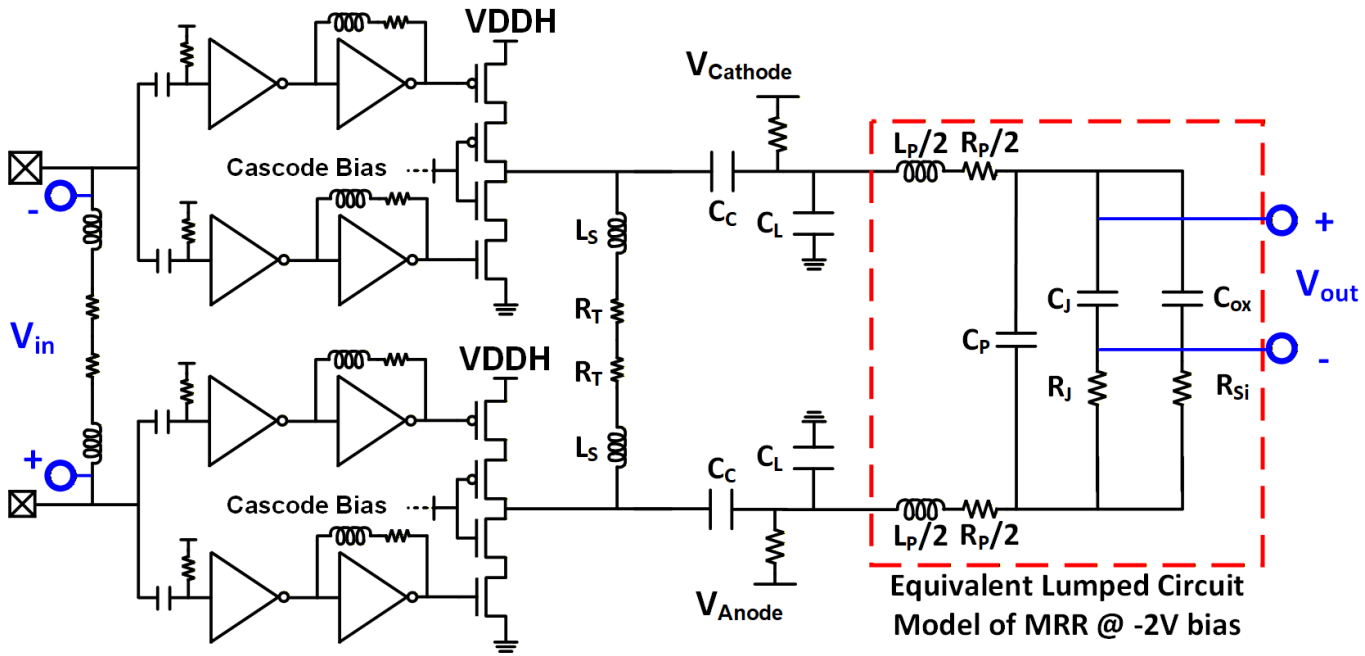
Eye	Width [UI]	Height [mV]
Top	Almost closed (<0.04 UI)	Almost closed (<10 mV)
Middle	Almost closed (<0.04 UI)	Almost closed (<10 mV)
Bottom	Almost closed (<0.04 UI)	Almost closed (<10 mV)



Eye	Width [UI]	Height [mV]
Top	0.376	60.2
Middle	0.384	61.4
Bottom	0.383	66.7

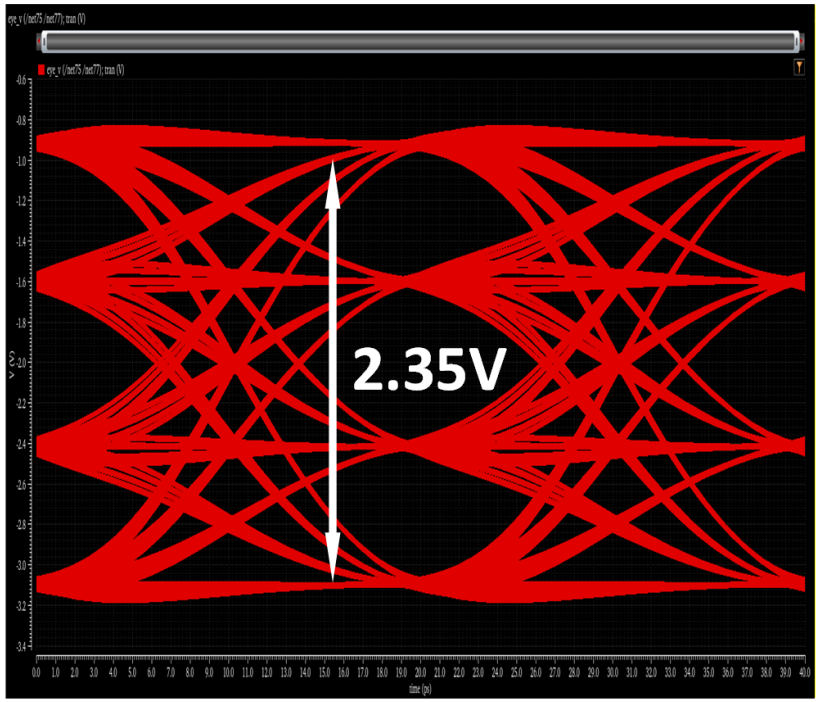
- The TX achieved 16 Gb/s/pin with 40.3 mV eye height at 1.6 pJ/b while compensating for PAM4 FEXT signals produced by two aggressors.
- To address the delay mismatches between the victim and the aggressors, I introduced delay adjustment circuits for PAM4 FEXT compensation for the first time.

3) 100 Gb/s Microring Modulator Driver (Ongoing)



MRR Driver schematic Design

R_T	40Ω
L_S	200pH
C_C	2pF
R_B	40kΩ
C_L	50fF
L_P	45.92pH
R_P	1.851Ω
C_P	20.16fF
R_J	196.5Ω
C_J	13.55fF
R_{Si}	2.611kΩ
C_{ox}	3.7fF



- The output driver uses a differential ac-coupled architecture to maximize output voltage and decouple it from MRM bias by utilizing on-chip bias-T.
- The output driver consists of a pseudo-differential stacked push-pull output stage to deliver 2.35 V_{ppd} output swing while satisfying the electrical overstress requirements.
- Inverter-based cherry-hooper amplifier are used the pre-driver to enhance the bandwidth.